Redlog: System Description for SMT-COMP 2017

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Redlog [1] is a key component of the open-source computer algebra system Reduce. It supplements Reduce's comprehensive collection of methods from symbolic computation with 100+ functions operating on formulas in interpreted first-order logic. Formulas co-exist and share data structures with conventional objects of symbolic computation within one homogeneous system. Within a rich infrastructure of methods on first-order formulas, Redlog has a strong focus on quantifier elimination and decision procedures for various algebraic theories.

We use here a simple wrapper to check satisfiability over real closed fields. In contrast to another configuration supporting a *read-eval-print loop (REPL)* for a subset of the SMT-LIB language, providing, e.g., *models* and *unsat cores*, this allows us to make use of specialized elimination algorithms and optimizations that are technically not SMT-ready yet, including virtual substitution (VS) up to degree three [3]. The above-mentioned REPL takes part in SMT-COMP 2017 in combination with the veriT SMT solver.

Redlog participates in the following divisions: LRA NRA.

References

1. A. Dolzmann and T. Sturm. Redlog: Computer algebra meets computer logic. *ACM SIGSAM Bulletin*, 31(2):2–9, 1997.
2. A. Dolzmann and T. Sturm. Simplification of quantifier-free formulae over ordered fields. *J. Symb. Comput.*, 24(2):209–231, 1997.
3. M. Košta. *New Concepts for Real Quantifier Elimination by Virtual Substitution.* Doctoral dissertation, Saarland University, Germany, December 2016.

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[*] The author order is strictly alphabetic.

[4] Repository at https://sourceforge.net/p/reduce-algebra/code/HEAD/tree/