ABC enters SMT competitions 2016. System description.

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Abstract. ABC [1] system is an industrial strength academic logic synthesis and verification tool, based on the And-Inverter Graphs (AIGs). It is augmented with powerful combinational bit-level verification engines, and in conjunction with the recently developed word-level front-end it could be used as a basic QF_BV SMT solver (i.e., SMT solver over the theory of quantifier-free bitvectors).

1 System Description

Two solver versions are submitted to the QF_BV section of the main track of SMT competitions 2016. The first one (default) is solely based on ABC and invokes internal engines for underlying satisfiability queries. The second one (glucose) uses an interface of Glucose [2] SAT solver.

References

1. Robert K. Brayton and Alan Mishchenko. *ABC: An Academic Industrial-Strength Verification Tool. Proceedings International Conference on Computer Aided Verification* (CAV), 2010.
2. Gilles Audemard and Laurent Simon. *Refining restarts strategies for SAT and UNSAT formulae. Proceedings International Conference on Principles and Practice of Constraint Programming* (CP), 2012.