veriT: System Description for SMT-COMP 2015

David Déharbe[1], Pablo Federico Dobal[2], and Pascal Fontaine[2]

[1] Universidade Federal do Rio Grande do Norte, Natal, RN, Brazil
`david@dimap.ufrn.br`
[2] LORIA–INRIA, Nancy, France
{`Pablo.Dobal, Pascal.Fontaine`}`@inria.fr`

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veriT is a satisfiability modulo theory (SMT) solver jointly developed by University of Lorraine, Inria (Nancy, France) and Federal University of Rio Grande do Norte (Natal, Brazil). veriT provides an open, trustable and reasonably efficient decision procedure [1] for the logic of unquantified formulas over uninterpreted symbols, linear real arithmetics, and the combination thereof. It also handles linear arithmetics over integers, and has quantifier reasoning using E-matching. Finally, veriT includes is proof-producing [3].

veriT is written in C and accepts the input formats SMT-LIB 2.0 and DIMACS. It integrates a DPLL-based Boolean satisfiability engine with a Nelson-Oppen like combination of decision and semi-decision procedures with propagation of model equalities, and implements simplifications such as symmetry-based reductions [2]. The tool is open-source and distributed under the BSD licence.

Since SMT-COMP 2014, the congruence closure decision procedure in veriT has been rewritten from scratch, and incremental improvements have been applied to the linear arithmetics reasoning engine. Ongoing developments include improving combination inside the solver, support for non-linear arithmetics, integers and quantifier reasoning.

veriT participates in the following divisions: QF_UF, QF_RDL, QF_LRA, QF_UFLRA, QF_IDL, QF_LIA, QF_UFLIA, AUFLIA, AUFLIRA.

References

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