

# System Description: Yices 2.2

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## Description

Yices 2.2 is the latest release in the Yices family of SMT solvers, developed by SRI International. Yices relies on the classical approach to SMT solving. It combines a CDCL-based Boolean satisfiability solver, with theory solvers for arrays, uninterpreted functions, and linear arithmetic. Yices also supports the theory of bitvectors via bit-blasting.

Yices 2.2 is the first version of Yices to support the SMT-LIB 2.0 notation, in addition to its own input language and to SMT-LIB 1.2. Yices 2.2 currently supports all the SMT-LIB 2.0 logics that do not require quantifiers or non-linear arithmetic. Yices supports most features of SMT-LIB 2.0, except the construction of unsatisfiable cores and the generation of proofs.

In SMT-COMP 2014, Yices will participate in all the quantifier-free divisions that do not include non-linear arithmetic. Yices will enter both the main track and the application track.

Yices is distributed at <http://yices.csl.sri.com>. It is free for research and other non-commercial uses. The solver is available in binary form for common operating systems such as Linux, Windows, Mac OS X, and FreeBSD.

A more complete description of Yices 2's architecture, solvers, and theory-combination algorithms will be presented at the CAV 2014 conference [1].

## References

1. Bruno Dutertre. Yices 2.2. In Armin Biere and Roderick Bloem, editors, *Computer-Aided Verification (CAV'2014)*, volume 8559 of *Lecture Notes in Computer Science*, pages 737–744. Springer, July 2014.